AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) A method for accessing a device by a host using a dedicated bus, the device having up to 2^M memory locations, the bus having N data lines and at least two control lines, wherein M is greater than N, and the host performs an address cycle by asserting a first control signal and a data cycle by de-asserting the first control signal, comprising:

(a) performing a first address cycle to transmit a first address portion over the bus during the first address cycle;

(b) storing the first address portion in a first register of the device in response to detecting the first address cycle;

(c) performing a second address cycle to transmit a second address portion over the bus during the second address cycle;

(d) storing the second address portion in a second register of the device in response to detecting the second address cycle;

(e) performing a first data cycle if the first and second address portions, when combined, form a first address for one of the memory locations;

(f) if the first data cycle is a write data cycle, transmitting a first datum from the host to the device during the first data cycle, and storing the first datum at the first address in response to detecting the first data cycle; and

(g) if the first data cycle is a read data cycle, transmitting a second datum from the device to the host during the first data cycle in response to detecting the first data cycle, the second datum being stored at the first address, wherein the second address cycle is immediately subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle.

2. (previously presented) The method of claim 1, wherein N equals eight and M equals sixteen.

3. (currently amended) The method of claim 1, further comprising, if the first and second address portions, when combined, are insufficient to form a first address:

(a) performing a third address cycle to transmit a third address portion over the bus during the third address cycle;

(b) storing the third address portion in a third register of the device in response to detecting the third address cycle; and

(c ~~e~~) performing the first data cycle if the first, second, and third address portions, when combined, form a first address for one of the memory locations, wherein the third address cycle is immediately subsequent to the second address cycle, and the first data cycle is immediately subsequent to the third address cycle.

4. (cancelled)

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9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (currently amended) A device, comprising:

at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in a memory space having 2^M addresses, each register associated with a particular count of address-bytes received on a dedicated bus for coupling the device and a processor, the bus having N data lines and at least two control lines, where M is greater than N;

a memory having a plurality of memory locations; and

a unit to monitor control signals placed on the bus by the processor, the unit including:

(a) a K-bit address-byte-received counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on a

first control line, wherein the number of the at least two registers is less than or equal to 2^K,

(b) a selecting unit to select one of the at least two registers according to a count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter,

(c) first logic to store an address-byte received on the bus in a currently selected register and to combine address-bytes stored in the at least two registers to form an address for one of the memory locations in response to detecting an assertion of the address transfer signal, and

(d) second logic to store a data-byte received on the bus at the address in response to detecting a de-assertion of the address transfer signal and assertion of a write signal, to fetch a data-byte stored at the address from the memory in response to detecting a de-assertion of the address transfer signal and assertion of a read signal, and to reset the address-byte received counter in response to detecting a de-assertion of the address transfer signal and assertion of one of the write or read signals.

13. (previously presented) The apparatus of claim 12, wherein N equals eight and M equals sixteen.

14. (cancelled)

15. (cancelled)

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (previously presented) A machine readable medium embodying a program of instructions for execution by a machine to perform a method for accessing a device by a host using a dedicated bus, the device having up to 2^M memory locations, the bus having N data lines and at least two control lines, wherein M is greater than N, and the host performs an address cycle by asserting a first control signal and a data cycle by de-asserting the first control signal, comprising:

(a) performing a first address cycle to transmit a first address portion over the bus during the first address cycle;

(b) storing the first address portion in a first register of the device in response to detecting the first address cycle;

(c) performing a second address cycle to transmit a second address portion over the bus during the second address cycle;

(d) storing the second address portion in a second register of the device in response to detecting the second address cycle;

(e) performing a first data cycle if the first and second address portions, when combined, form a first address for one of the memory locations;

(f) if the first data cycle is a write data cycle, transmitting a first datum from the host to the device during the first data cycle, and storing the first datum at the first address in response to detecting the first data cycle; and

(g) if the first data cycle is a read data cycle, transmitting a second datum from the device to the host during the first data cycle in response to detecting the first data cycle, the second datum being stored at the first address, wherein the second address cycle is immediately subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle.

24. (previously presented) The machine readable medium of claim 23, wherein N equals eight and M equals sixteen.

25. (currently amended) The machine readable medium of claim 23, further comprising, if the first and second address portions, when combined, are insufficient to form a first address:

(a) performing a third address cycle to transmit a third address portion over the bus during the third address cycle;

(b) storing the third address portion in a third register of the device in response to detecting the third address cycle; and

(c ~~b~~) performing the first data cycle if the first, second, and third address portions, when combined, form a first address for one of the memory locations, wherein the third address cycle is immediately subsequent to the second address cycle, and the first data cycle is immediately subsequent to the third address cycle.

26. (cancelled)

27. (cancelled)

28. (cancelled)

29. (cancelled)

30. (cancelled)

31. (cancelled)

32. (cancelled)

33. (cancelled)

34. (cancelled)

35. (cancelled)

36. (cancelled)

37. (currently amended) A system, comprising:

a central processing unit;

a device having:

at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in a memory space having 2^M addresses;

a memory having a plurality of memory locations;

a unit to monitor control signals placed on the bus by the central processing unit, the unit including:

(a) a K-bit address-byte-received counter to count address-bytes received on a bus by counting each assertion of an address transfer signal on a first control line, wherein the number of the at least two registers is less than or equal to 2^K,

(b) a selecting unit to select one of the at least two registers according to a count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter,

(c) first logic to store an address-byte received on the bus in a currently selected register and to combine address-bytes stored in the at least two registers to form an address for one of the memory locations in response to detecting an assertion of the address transfer signal, and

(d) second logic to store a data-byte received on the bus at the address in response to detecting a de-assertion of the address transfer signal and assertion of a write signal, to fetch a data-byte stored at the address from the memory in response to detecting a de-assertion of the address transfer signal and assertion of a read signal, and to reset the address-byte received counter in response to detecting a de-assertion of the address transfer signal and assertion of one of the write or read signals; and

the bus to exclusively couple the central processing unit and the device, the bus having N data lines and at least two control lines, where M is greater than N.

38. (previously presented) The system of claim 37, wherein N equals eight and M equals sixteen.

39. (cancelled)

40. (cancelled)

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42. (cancelled)

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46. (cancelled)

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49. (cancelled)

50. (cancelled)